ZILKA·KOTAB
PC
ZILKA, KOTAB & FEECE™

100 PARK CENTER PLAZA, SUITE 300
SAN JOSE, CA 95113

TELEPHONE (408) 971-2573
FAX (408) 971-4660

FAX COVER SHEET

Date: January 18, 2006	Phone Number	Fax Number
To: Board of Patent Appeals & Interferences		(571) 273-8300
From: Kevin J. Zilka		

Docket No.: NVIDP064/P000286 **App. No: 10/006,551**

Total Number of Pages Being Transmitted, Including Cover Sheet: 27

Message:

Please deliver to the Board of Patent Appeals & Interferences.

Thank you,

Kevin J. Zilka

☐ *Original to follow Via Regular Mail* X *Original will Not be Sent* ☐ *Original will follow Via Overnight Courier*

IF YOU DO NOT RECEIVE ALL PAGES OR IF YOU ENCOUNTER
ANY OTHER DIFFICULTY, PLEASE PHONE Erica
AT (408) 971-2573 AT YOUR EARLIEST CONVENIENCE

RECEIVED
CENTRAL FAX CENTER

JAN 18 2006

Practitioner's Docket No. NVIDP064/P000286 *PATENT*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: C. Donham et al.

Application No.: 10/006,551 Group No.: 2676
Filed: 11/30/2001 Examiner: Tran, T.
For: SYSTEM, METHOD AND COMPUTER PROGRAM PRODUCT FOR USING TEXTURES AS INSTRUCTIONS FOR GRAPHICS PROCESSING

Mail Stop Appeal Briefs – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF
(PATENT APPLICATION--37 C.F.R. § 41.37)

1. Transmitted herewith, is the APPEAL BRIEF in this application, which is in furtherance of a second Notice of Appeal, filed in this case on November 18, 2005, thereby re-instating the appeal originally initiated by the filing of a first Notice of Appeal, filed in this case on March 09, 2004.

2. STATUS OF APPLICANT

This application is on behalf of other than a small entity.

CERTIFICATION UNDER 37 C.F.R. §§ 1.8(a) and 1.10*
(When using Express Mail, the Express Mail label number is mandatory; Express Mail certification is optional.)

I hereby certify that, on the date shown below, this correspondence is being:

MAILING

_ deposited with the United States Postal Service in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

37 C.F.R. § 1.8(a)
_ with sufficient postage as first class mail.

37 C.F.R. § 1.10*
_ as "Express Mail Post Office to Addressee"
Mailing Label No. _____ **(mandatory)**

TRANSMISSION
✓ facsimile transmitted to the Patent and Trademark Office, (571) 273 - 8300.

Date: 1/18/06

Signature

Erica L. Farlow
(type or print name of person certifying)

** Only the date of filing (' 1.6) will be the date used in a patent term adjustment calculation, although the date on any certificate of mailing or transmission under ' 1.8 continues to be taken into account in determining timeliness. See ' 1.703(f). Consider "Express Mail Post Office to Addressee" (' 1.10) or facsimile transmission (' 1.6(d)) for the reply to be accorded the earliest possible filing date for patent term adjustment calculations.*

RECEIVED
CENTRAL FAX CENTER

JAN 18 2006

3. FEE FOR FILING APPEAL BRIEF

Pursuant to 37 C.F.R. §1.17(c), the fee for filing the Appeal Brief has already been paid. However, the Commissioner is authorized to charge any fees that may be due to deposit account 50-1351 (NVIDP064).

4. EXTENSION OF TERM

The proceedings herein are for a patent application and the provisions of 37 C.F.R. § 1.136 apply.

Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

Current Appeal brief fee	$500.00
Appeal brief fee	$330.00 (previously paid on April 30, 2004)
Total Fee Due	$170.00

6. FEE PAYMENT

Authorization is hereby made to charge the amount of $170.00 to Deposit Account No. 50-1351 (Order No. NVIDP064).

A duplicate of this transmittal is attached.

7. FEE DEFICIENCY

If any additional extension and/or fee is required, and if any additional fee for claims is required, charge Deposit Account No. 50-1351 (Order No. NVIDP064).

Reg. No.: 41,429
Tel. No.: 408-971-2573
Customer No.: 28875

Signature of Practitioner
Kevin J. Zilka
Zilka-Kotab, PC
P.O. Box 721120
San Jose, CA 95172-1120
USA

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of C. Donham et al. Application No. 10/006,551 Filed: November 30, 2001 For: SYSTEM, METHOD AND COMPUTER PROGRAM PRODUCT FOR USING TEXTURES AS INSTRUCTIONS FOR GRAPHICS PROCESSING	Examiner: Tran, Tam D. Art Unit: 2676 Docket: NVIDP064/P000286 Date: January 18, 2006

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ATTENTION: Board of Patent Appeals and Interferences

APPELLANT'S BRIEF (37 C.F.R. § 41.37)

This brief is in furtherance of a second Notice of Appeal, filed in this case on November 18, 2005, thereby re-instating the appeal originally initiated by the filing of a first Notice of Appeal, filed in this case on March 09, 2004.

The fees required under § 1.17, and any required petition for extension of time for filing this brief and fees therefor, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains these items under the following headings, and in the order set forth below (37 C.F.R. § 41.37(c)(i)):

I REAL PARTY IN INTEREST

01/20/2006 NNGUYEN1 00000002 501351 10006551
01 FC:1402 170.00 DA 330.00 OP

Adjustment date: 01/20/2006 NNGUYEN1
05/05/2004 MGEBREM1 00000147 10006551
01 FC:1402 -330.00 OP

II RELATED APPEALS AND INTERFERENCES

III STATUS OF CLAIMS

IV STATUS OF AMENDMENTS

V SUMMARY OF CLAIMED SUBJECT MATTER

VI ISSUES

VII ARGUMENTS

VIII APPENDIX OF CLAIMS INVOLVED IN THE APPEAL

IX APPENDIX LISTING ANY EVIDENCE RELIED ON BY THE APPELLANT IN THE APPEAL

The final page of this brief bears the practitioner's signature.

I REAL PARTY IN INTEREST (37 C.F.R. § 41.37(c)(1)(i))

The real party in interest in this appeal is NVIDIA Corporation.

II RELATED APPEALS AND INTERFERENCES (37 C.F.R. § 41.37(c)(1)(ii))

With respect to other prior or pending appeals, interferences, or related judicial proceedings that will directly affect, or be directly affected by, or have a bearing on the Board's decision in the pending appeal, there are no other such appeals, interferences, or related judicial proceedings.

Since no such proceedings exist, no Related Proceedings Appendix is appended hereto.

III STATUS OF CLAIMS (37 C.F.R. § 41.37(c) (1)(iii))

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

Claims in the application are: 1-30

B. STATUS OF ALL THE CLAIMS IN APPLICATION

1. Claims withdrawn from consideration: none
2. Claims pending: 1-30
3. Claims allowed: None
4. Claims rejected: 1-30

C. CLAIMS ON APPEAL

The claims on appeal are: 1-30

See additional status information in the Appendix of Claims.

IV STATUS OF AMENDMENTS (37 C.F.R. § 41.37(c)(1)(iv))

As to the status of any amendment filed subsequent to final rejection, no such amendments exist.

V SUMMARY OF CLAIMED SUBJECT MATTER (37 C.F.R. § 41.37(c)(1)(v))

With respect to a summary of Claims 1, 24, and 26-30, as shown in Figures 3A and 5 and the accompanying descriptions on pages 9-11 and 12-13, a system and method are provided for retrieving instructions from video memory (e.g. see item 304 of Figure 3A, for example, etc.) utilizing a texture module (e.g. see item 301 of Figure 3A, for example, etc.) in a graphics pipeline. During use, an instruction request is sent to the video memory utilizing the texture module in the graphics pipeline. In response thereto, instructions are received from the video memory in response to the instruction request utilizing the texture module in the graphics pipeline.

With respect to a summary of Claim 25, the above summary is incorporated herein by reference, at least in part. Further, as shown in Figures 3A and 5 and the accompanying descriptions on pages 9-11 and 12-13, a system is provided for retrieving instructions from video memory. Such system includes a means (e.g. see items 301 and/or 303 of Figure 3A, for example, etc. described on pages 9-11) for sending an instruction request to video memory. Further included is a means (e.g. see items 301 and/or 303 of Figure 3A, for example, etc. described on pages 9-11) for receiving instructions from the video memory in response to the instruction request.

VI ISSUES (37 C.F.R. § 41.37(c)(1)(vi))

Following, under each issue listed, is a concise statement setting forth the corresponding ground of rejection.

Issue # 1: The Examiner has rejected Claims 1, 4, 5, 8, 9, 18-21, 24-27 and 30 under 35 U.S.C. 102(b) as being anticipated by Peterson et al. (U.S.P.N. 5767856).

Issue # 2: The Examiner has further rejected Claims 2, 3, 6, 7, 10-17, 22, 23, 28, 29 under 35 U.S.C. 103(a) as being unpatentable over Peterson et al. (U.S.P.N. 5767856) in view of Appellant's Admitted Prior Art (AAPA).

VII ARGUMENTS (37 C.F.R. § 41.37(c)(1)(vii))

The claims of the groups noted below do not stand or fall together. In the present section, appellant explains why the claims of each group are believed to be separately patentable.

Issue #1:

The Examiner has rejected Claims 1, 4, 5, 8, 9, 18-21, 24-27 and 30 under 35 U.S.C. 102(b) as being anticipated by Peterson et al. (U.S.P.N. 5767856).

Group #1: Claims 1, 8, 9, 20-21, 24-27, and 30

With respect to the present grouping, the Examiner has relied on Figure 2 and the following excerpt from Peterson, at least in part, to make a prior art showing of appellant's claimed "sending an instruction request to video memory utilizing a texture module" (see this or similar, but not identical, language in each of the foregoing claims).

> "The pixel engine pipeline is an in-order pipeline. In other words, instructions from the processor are acted upon in the order that they are issued. From the command queue, commands and direct data are sent to attribute queue 220. These commands include instructions as to how many bytes should be retrieved from the read data queue 245. Read requests are sent to read request queue 230 for subsequent use by D-cache 130. The read request is in the form of an address and a number of bytes to read. Example of data that might need to be read includes Z, texel, and pixel information. Control logic 255 within the data block determines whether or not the data has to actually be retrieved from the system memory 170." (Col. 3, lines 62-67; col. 4, lines 1-6)

Per the Examiner's Response to Arguments, the Examiner now relies on Peterson's "read data queue" (see excerpt above and Fig. 2, item 230) to meet appellant's claimed "video memory."

Examiner goes on to rely on Figure 2 and the following excerpt from Peterson, at least in part, to make a prior art showing of appellant's claimed "receiving instructions from the video memory in response to the instruction request utilizing the texture module in the graphics pipeline" (see this or similar, but not identical, language in each of the foregoing claims).

> "The information in the attribute queue is extracted in a first-in-first-out basis to continue down the pixel pipeline for processing by the functional units of the pixel engine. As discussed above, at the time read requests were made, instructions were placed in the attribute queue as to how to extract data from read data queue 245. As these instructions are encountered when processing the contents of the attribute queue, control logic 265 extracts information from the read data queue to send down the pixel pipeline." (Col. 4, lines 59-67)

Specifically, the Examiner points to Peterson's "attribute queue" as receiving instructions to output from a pixel pipeline. The only source of instructions for the "attribute queue" (see excerpt above and Fig. 2, item 220), however, is the command queue 210.

By making such arguments, the Examiner has relied on at least two completely different entities in Peterson to meet appellant's claimed "video memory." Note claim chart below in Table 1:

Table 1

Appellant's claimed language	Peterson's disclosure
video memory	1) read data queue 230 2) command queue 210

Appellant respectfully disagrees with this approach, since by proceeding in such manner, it appears that the Examiner has simply broken down appellant's claim language into components (i.e. phrases, adjectives, nouns, etc.), and has then attempted to make a prior art showing of such components in a vacuum. Thus, the

Examiner's rejection may be considered analogous to gleaning phrases, adjectives, nouns, etc. from appellant's claims, and then using the prior art reference collectively as a dictionary to make a prior art showing of only the terms of the claimed subject matter.

This is inherently inappropriate since, in order for a claim to be anticipated, the elements must be *arranged* as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

Specifically, since the Examiner uses a first Peterson feature (e.g. read data queue 230, etc.) to meet a claim element (e.g. video memory, etc.) in a first context in the claims, and then uses a second different Peterson feature (e.g. command queue 210, etc.) to meet the same claim element (e.g. video memory, etc.) in a different second context in the claims (as noted above), appellant's claim elements are simply not *arranged* as required by the claims.

To this end, the aforementioned anticipation requirement has not been met, at least for the reasons set forth above.

Further, the Examiner's random use of the terms in the prior art reference is further evidence that the Peterson reference fails to *enable* the claimed invention. The disclosure in an assertedly anticipating reference must provide an enabling disclosure of the desired subject matter; mere naming or description of the subject matter is insufficient, if it cannot be produced without undue experimentation. *Elan Pharm., Inc. v. Mayo Foundation for Medical and Education Research,* 346 F.3d 1051, 1054, 68 USPQ2d 1373, 1376 (Fed. Cir. 2003). Further, as held in *Paperless Accounting, Inc. v. Bay Area Rapid Transit Systems*, 804 F.2d 659, 665, 231 USPQ 649, 653 (Fed. Circ. 1986): "[A] § 102(b) reference must sufficiently describe the claimed invention to have placed the public possession of it...[E]ven is the claimed invention is disclosed in a printed publication, that disclosure will not suffice as prior art if it was not enabling...". See also, Akzo N.V. v. U.S.I.T.C., 808 F.2d

1479, 1 USPQ2d 1241, 1245 (Fed.Cir. 1986) ("the prior art reference must be enabling...").

It is simply unreasonable to assume that one of ordinary skill would be able to identify the cryptic "mapping" of Table 1 above, so as to identify and enable the claimed invention, without undue experimentation.

Again, the aforementioned anticipation requirement has not been met, at least for the reasons set forth above.

Most importantly, the Examiner's rejection is faulty, since each and every element as set forth in the claim has not been found.

Again, the Examiner relies on Peterson's "read data queue" (see excerpt above and Fig. 2, item 230) to meet appellant's "video memory" in the claimed "sending an instruction request to video memory utilizing a texture module." However, the read data queue 230 of Peterson is only adapted to be sent "read requests" to initiate reading "Z, texel, and pixel information." Thus, Peterson's "read requests" clearly do not meet appellant's claimed "instruction requests," since Peterson's "read requests" merely request "Z, texel, and pixel information," and not instructions, as claimed by appellant.

In a similar vein, the Examiner relies on Peterson's "attribute queue" to meet the claimed "receiving instructions from the video memory in response to the instruction request utilizing the texture module in the graphics pipeline." Again, the only source of instructions for the "attribute queue" (see excerpt above and Fig. 2, item 220), however, is the command queue 210. Such "command queue 210," however, fails to meet appellant's claimed "video memory."

Further, instructions are not received from the "command queue 210" in response to the instruction request utilizing the texture module in the graphics pipeline, let alone

where such instruction request is sent to video memory utilizing a texture module, as claimed.

Yet again, the aforementioned anticipation requirement has not been met.

By retrieving the instructions utilizing the texture module, much pipeline bandwidth is saved at the input of the texture module, since prior art configuration data at least in part need not necessarily be received from the rasterizer. Moreover, the memory traditionally employs a high-bandwidth connection with the texture module, which may be used for efficient retrieval of the instructions.

The instructions may then be used by the texture module in order to control various graphics processing involving the texels, pixels, and/or primitives, etc. For example, the instructions may control how subsequent texels may be mapped to pixels associated with primitives. Moreover, the instructions may be used to control the mapping, or blending, of the texels with the pixels, in accordance with the instructions. Simply nowhere in the prior art is there such a combination of features for fulfilling the foregoing objectives.

It is finally noted that, in the latest Office Action mailed 09/30/05, the Examiner alleges that appellant argues that the prior art fails to teach an "instruction set." In response, appellant emphasizes that such arguments were made not with respect to the independent claims, but rather the dependent claims, as noted below.

Group #2: Claim 4-5

With respect to the current grouping, the Examiner has relied on the following excerpt and Figure 1 of Peterson, respectively, to make a prior art showing of appellant's claimed technique "wherein the video memory includes a frame buffer" (Claim 4) and "wherein the video memory includes direct random access memory (DRAM)" (Claim 5).

> "A data flow diagram for the output end of the pixel engine pipeline is illustrated in FIG. 3. The output of the pixel engine will eventually be sent to system memory or the video buggers (154 in FIG. 1)." (Col. 5, lines 3-7)

Appellant respectfully asserts that the above excerpt and Figure 1 from Peterson teach that the output from the pixel engine is sent to memory. However, the "video memory" in appellant's foregoing claims relates to where the instruction request is sent, and not simply to where output of an entire pixel engine is sent. Furthermore, the instructions in Peterson are only sent to the attribute queue (see Col. 3, lines 63-66), and thus are NOT sent to a frame buffer or DRAM, in the manner claimed by appellant.

Again, the aforementioned anticipation requirement has not been met.

Group #3: Claim 18-19

With respect to dependent Claims 18-19, the Examiner has simply relied on Figure 2 of Peterson to make a prior art showing of appellant's claimed technique "wherein a complete instruction set is received in response to the instruction request" (Claim 18) and "wherein a partial instruction set is received in response to the instruction request" (Claim 19).

Appellant respectfully asserts that nowhere in Figure 2 is there any disclosure of an "instruction set," either complete or partial, as claimed by appellant. All Peterson discloses with respect to instructions is that commands are sent from the command queue to the attribute queue, where "[t]he commands include instructions as to how many bytes should be retrieved from the read data queue 245" (see Col. 3, lines 63-66). Thus, there is clearly no disclosure of receiving "instruction sets," in the manner claimed by appellant.

Again, the aforementioned anticipation criterion has simply not been met by the Examiner's reference.

Issue #2

The Examiner has further rejected Claims 2, 3, 6, 7, 10-17, 22, 23, 28, and 29 under 35 U.S.C. 103(a) as being unpatentable over Peterson et al. (U.S.P.N. 5767856) in view of Appellant's Admitted Prior Art (AAPA).

Group #1: Claims 2, 3, 6, 7, 10-17, 22, 23, 28, and 29

Such claims depend from the independent claims addressed under Group #1 of Issue #1 or are deemed allowable by virtue of similar deficiencies with respect to the anticipation requirements set forth hereinabove. To this end, such claims are deemed allowable by virtue of the foregoing arguments.

In view of the remarks set forth hereinabove, all of the independent claims are deemed allowable, along with any claims depending therefrom.

VIII APPENDIX OF CLAIMS (37 C.F.R. § 41.37(c)(1)(viii))

The text of the claims involved in the appeal (along with associated status information) is set forth below:

1. (Previously Presented) A method for retrieving instructions from video memory utilizing a texture module in a graphics pipeline, comprising:
   (a) sending an instruction request to video memory, where a texture module in a graphics pipeline sends the instruction request to the video memory; and
   (b) receiving instructions from the video memory in response to the instruction request utilizing the texture module in the graphics pipeline.

2. (Previously Amended) The method as recited in claim 1, and further comprising sending a texture request to video memory utilizing the texture module in the graphics pipeline.

3. (Previously Amended) The method as recited in claim 2, and further comprising receiving texture information from the video memory in response to the texture request utilizing the texture module in the graphics pipeline.

4. (Previously Amended) The method as recited in claim 1, wherein the video memory includes a frame buffer.

5. (Previously Amended) The method as recited in claim 4, wherein the video memory includes direct random access memory (DRAM).

6. (Original) The method as recited in claim 3, wherein the instructions are adapted for controlling a texture environment module coupled to the texture module.

7. (Original) The method as recited in claim 6, wherein the instructions control the manner in which the texture environment module processes the texture information.

8. (Original) The method as recited in claim 1, and further comprising receiving initial instructions from a rasterizer module coupled to the texture module.

9. (Original) The method as recited in claim 8, wherein the initial instructions control at least the sending of the instruction request by the texture module.

10. (Original) The method as recited in claim 3, and further comprising temporarily storing the instructions and the texture information in cache.

11. (Original) The method as recited in claim 10, wherein the cache is resident on the texture module.

12. (Previously Amended) The method as recited in claim 3, wherein each piece of texture information and each of the instructions are of a similar size in the video memory.

13. (Original) The method as recited in claim 3, and further comprising controlling the texture module utilizing a shader module coupled thereto.

14. (Original) The method as recited in claim 13, wherein the shader module controls the sending of the instruction request and the texture request by the texture module.

15. (Original) The method as recited in claim 13, wherein the shader module processes a plurality of pixels with the texture information based on the instructions.

16. (Previously Amended) The method as recited in claim 15, wherein the shader module is capable of reusing the texture information in order to request further texture information from the video memory.

17. (Original) The method as recited in claim 15, and further comprising ceasing the processing upon the receipt of a terminate instruction.

18. (Original) The method as recited in claim 1, wherein a complete instruction set is received in response to the instruction request.

19. (Original) The method as recited in claim 1, wherein a partial instruction set is received in response to the instruction request.

20. (Original) The method as recited in claim 19, and further comprising repeating (a) – (b) in accordance with the instructions.

21. (Original) The method as recited in claim 1, wherein (a) – (b) are carried out in accordance with the instructions received in response to the instruction request.

22. (Original) The method as recited in claim 1, wherein the texture module is adapted for operating in a plurality of different modes.

23. (Original) The method as recited in claim 22, wherein the instructions are received in a predetermined one or more of the different modes.

24. (Previously Presented) A computer program product for retrieving instructions from video memory utilizing a texture module in a graphics pipeline, comprising:

(a) computer code for sending an instruction request to video memory, where a texture module in a graphics pipeline sends the instruction request to the video memory; and

(b) computer code for receiving instructions from the video memory in response to the instruction request utilizing the texture module in the graphics pipeline.

25. (Previously Presented) A system for retrieving instructions from video memory utilizing a texture module in a graphics pipeline, comprising:

(a) means for sending an instruction request to video memory, where a texture module in a graphics pipeline sends the instruction request to the video memory; and

(b) means for receiving instructions from the video memory in response to the instruction request.

26. (Previously Presented) A texture module for retrieving instructions from video memory capable of carrying out a method, comprising:

(a) sending an instruction request to video memory, where the texture module sends the instruction request to the video memory; and

(b) receiving instructions from the video memory in response to the instruction request.

27. (Previously Presented) A data structure stored in a frame buffer of a graphics pipeline for allowing the retrieval of instructions, where a texture module coupled thereto sends the instruction request to video memory, the data structure comprising an instruction object stored in the frame buffer for being retrieved therefrom in response to the instruction request utilizing the texture module in the graphics pipeline.

28. (Previously Presented) A method for retrieving instructions from video memory, comprising:

(a) receiving a plurality of preliminary instructions from a rasterizer module utilizing a texture module coupled thereto;

(b) sending an instruction request to video memory, where the texture module sends the instruction request to the video memory;

(c) receiving additional instructions from the video memory in response to the instruction request utilizing the texture module;

(d) caching the additional instructions on the texture module;

(e) sending a texture request to video memory utilizing the texture module in accordance with the additional instructions;

(f) receiving texture information from the video memory in response to the texture request utilizing the texture module;

(g) caching the texture information on the texture module; and

(h) repeating (b) – (g) in accordance with the additional instructions.

29. (Previously Presented) A method for retrieving instructions from video memory, comprising:

(a) receiving a plurality of preliminary instructions from a rasterizer module utilizing a shader module coupled thereto;

(b) sending an instruction request to video memory, where a texture module coupled to the shader module sends the instruction request to the video memory;

(c) receiving additional instructions from the video memory in response to the instruction request utilizing the texture module;

(d) caching the additional instructions on the texture module;

(e) sending a texture request to video memory utilizing the texture module in accordance with the additional instructions;

(f) receiving texture information from the video memory in response to the texture request utilizing the texture module;

(g) caching the texture information on the texture module;

(h) processing a plurality of pixels with the texture information utilizing the shader module in accordance with the additional instructions;

(i) repeating (b) – (h) in accordance with the additional instructions; and

(j) outputting the processed pixels upon receipt of additional instructions that include a terminate instruction.

30. (Previously Presented) A method for retrieving instructions from video memory utilizing a cache in a graphics pipeline, comprising:

sending an instruction request to video memory in a graphics pipeline, where a cache in the graphics pipeline sends the instruction request to the video memory; and

receiving instructions from the video memory in response to the instruction request for storage in the cache in the graphics pipeline.

IX APPENDIX LISTING ANY EVIDENCE RELIED ON BY THE APPELLANT IN THE APPEAL (37 C.F.R. § 41.37(c)(1)(ix))

There is no such evidence.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 971-2573. For payment of any additional fees due in connection with the filing of this paper, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1351 (Order No. NVIDP064/P00286).

Respectfully submitted,

By: _____ Date: 1/18/06

Kevin J. Zilka

Reg. No. 41,429

Zilka-Kotab, P.C.
P.O. Box 721120
San Jose, California 95172-1120
Telephone: (408) 971-2573
Facsimile: (408) 971-4660